Submitted for publication in the IEEE Trans. on Nuclear Science December 1993 issue.

# ON-CHIP p-MOSFET DOSIMETRY

M. G. Buehler, B. R. Blaes, G. A, Soli, and G. R. Tardio
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, CA 91109

ABSTRACT

On-chip p-FETs were developed to monitor the radiation dose of n-well CMOS ICs by monitoring threshold voltage shifts due to radiation induced oxide and interface charge. The design employs closed geometry FETs and a zero-biased n-well to eliminate leakage currents. The FETs are operated using a constant current chosen to greatly reduce the FET's temperature sensitivity. The dose sensitivity of these p-FETs is about -2.6 mV/krad(Si) and the off-chip instrumentation resolves about 400 rad(Si)/bit. When operated with a current at the temperature-independent point, the output voltage, VO, is located near -1.5 V and depends only on silicon material parameters. Temperature effects are less than ±63 μV/°C over a 70°C temperature range.

## 1. INTRODUCTION

The use of FETs (Field-Effect Transistors) as dosimeters was pioneered by Holmes-Siedle [1]. A number of these devices have flown on earth bound satellites [2 - 4].

In recent. years, p-FET dosimeters have been developed with specially-grown thick-gate oxides which have a large number of oxide traps. Sensitivities of >10 mV/rad(Si) [5] have been achieved. The sensitivity to radiation can also be enhanced by applying a large positive bias during radiation which forces more of the positive oxide charge to the interface. The p-FET temperature sensitivity can be minimized by operating the p-FET with a current at the temperature-independent point [6, 7].

In this work, a p-FET dosimeter is developed under the constraint that the dosimeter be useful in predicting the radiation dose of an IC fabricated with a non-radiation hardened 1.2-μm CMOS process, As shown in Fig, 1, two p-FETs were fabricated on the RADMON (Radiation Monitor), which also includes an SEU-SRAM for monitoring particle upsets. This appears to be the first time a p-FET dosimeter was fabricated in a fine-line, thin-oxide semiconductor technology.

The p-FET is biased to about -1.5 V during measurement and is unbiased when not being measured. This approach to biasing is intended to provide a known bias environment at all times. In certain applications, the availability of spacecraft power is unpredictable. Thus being unbiased during irradiation, provides a known bias scenario.

On-chip dosimetry provides the advantage that the dose is measured directly next to the IC. This reduces the uncertainty inherent in dosimetry calculations which are complicated especially for highly shielded electronics.

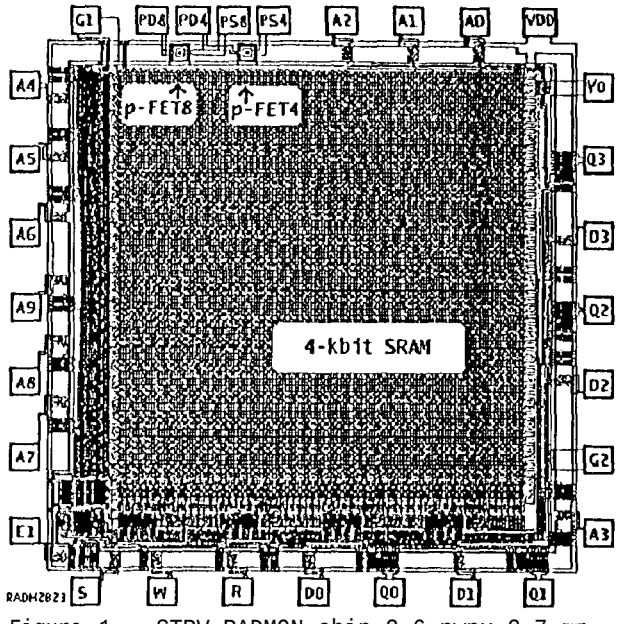


Figure 1. STRV-RADMON chip 2.6 nwnx 2.7 mm.

## 2. p-FET DESIGN

The RADMON, shown in Fig. 1, contains two p-FETs . The geometry of p-FET4 is W/l = 182/4 Urn/pm and p-FET8 is W/L = 182/8 μm/μm. The layout of the p-FET, shown in Fig. 2, features a closed geometry design where the drain is completely surrounded by the source. The closed geometry eliminates the bird's

beak leakage encountered in a linear FET. The schematic cross section of the device, shown in Fig. 3, indicates that the n-well and source are separated so they can operate at slightly different biases required by the first operational amplifier shown in the figure. Grounding the n-well is a departure from normal CMOS circuit operation where the n-well is normally connected to VDD.

In operation all terminals of the p-FET are operated near ground except the drain which operates near VO = -1.5 V. During irradiation, the device is biased in the off state. The two RL resistors are used to bleed off any charge remaining on the p-FET.

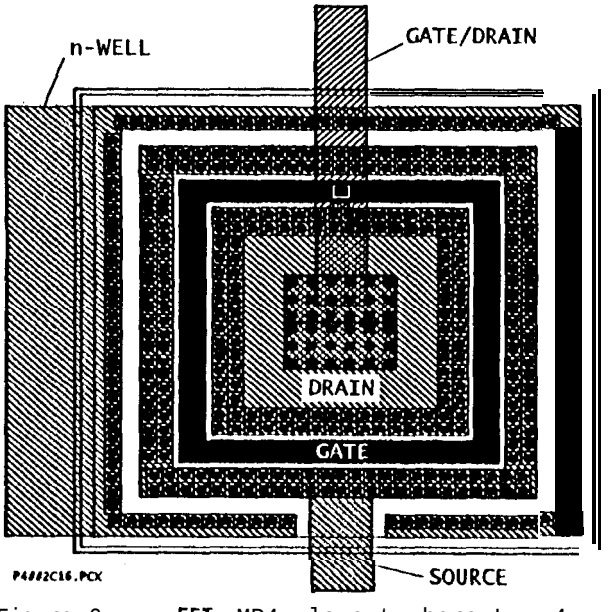


Figure 2. p-FET, MP4, layout where L = 4 $\mu$m and W = 182 $\mu$m.

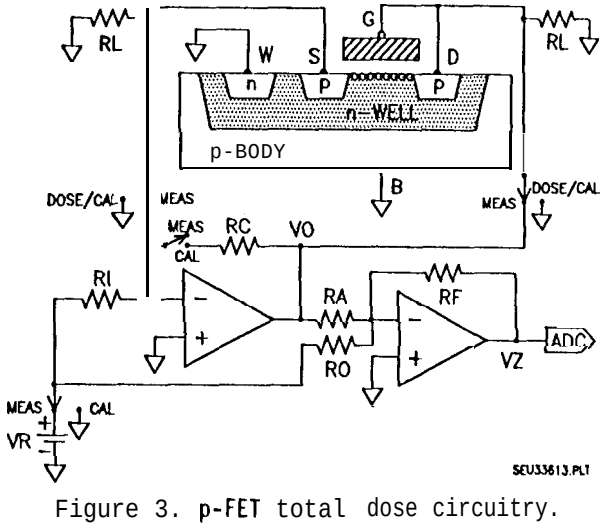


Figure 3. p-FET total dose circuitry.

The instrumentation is calibrated by replacing the p-FET with the RC resistor.

The p-FET constant drain current, ID, is established by VR and RI or ID = VR/RI. The output of the first operational amplifier is scaled by the second operational amplifier so that it makes maximum use of the range of the 8-bit ADC (Analog-to-Digital Converter). As seen in Fig. 3, the gate is connected to the drain. This insures that the p-FET is operated in the saturation region.

## 3. p-FET MODEL EQUATIONS

In saturation the p-FET drain current [7] is:

$$(1)\quad ID = \frac{\beta}{2}\cdot\frac{(-VO + VT)^2}{1 + \theta(-VO + VT)}$$

where VO is the p-FET output voltage, $\beta = KP\cdot W/L$, $KP = \mu_0\cdot C_0$ and VT is the p-FET threshold voltage. $W_e$ and $L_e$ are the effective channel width and length respectively, $\mu_0$ is the zero-field channel mobility, Co is the gate oxide capacitance per unit area, and $\theta$ is the mobility electric-field degradation parameter.

The above equation was simplified by taking its square root. Then the $\theta$ term was linearized using the Taylor Series expansion:

$$(2)\quad \sqrt{ID} = \sqrt{\beta/2}(-VO + VT)\left[1 - \frac{\theta}{2}(-VO + VT)\right]$$

Expressions for the temperature and dose dependence of VT, $\beta$, and $\theta$ are given below. The equations are expanded about the characterization or reference temperature To. In these equations, the temperature and dose effects are assumed to be independent. That is, the equations do not include a dose-temperature product term.

The threshold voltage is described by:

$$(3)\quad VT = VT_0 + VTT(T - To) + VT_D\cdot D$$

where $VT_0$ is the threshold voltage at To, $VTT = \partial VT/\partial T|_{T\to To}$ and $VTD = \partial VT/\partial D|_{D\to 0}$. The temperature [7] and dose dependence [8] of $\beta$ is given by:

$$(4)\quad \beta = \beta_0(T/T_0)^{-n} + \beta_D\cdot D$$

where $\beta_0$ is $\beta$ evaluated at $T_0$, $\beta_D = \partial\beta/\partial D|_{D\to 0}$, n characterizes the mobility temperature dependence, and T is the absolute temperature. For $D_T = \partial D/\partial T = 0$:

(5) $\beta_T = \partial\beta/\partial T = -n \cdot \beta/T$

The temperature and dose dependence of θ is given by:

(6) $\theta = \theta_0 + \theta_T \cdot (T - To) + \theta_D \cdot D$

where $\theta_0$ is e evaluated at To, $\theta_T = \partial\theta/\partial T|_{T \to To}$ and $\theta_D = \partial\theta/\partial D|_{D \to 0}$.

## 4. p-FET TEMPERATURE EQUATIONS (INCLUDING θ)

In this section the p-FET equations are derived including the θ parameter. This allows an accurate analysis at the operating or measurement temperature, $T_m$. This temperature is usually different from the characterization temperature, To. The measurement temperature, $T_m$, might be the mean operating temperature for a spacecraft.

The p-FET output voltage follows from Eq. 2. The solution requires solving the quadratic equation in VO:

(7) $VO = VT - \frac{1}{\theta} \cdot (1 - \sqrt{1 - \theta \cdot \sqrt{[8 \cdot ID/\beta]}})$

The sign of the square root is negative which can be verified by evaluating this equation at θ = 0.

The current, $ID_m$, at the measurement temperature is found from the above equation by setting $\partial VO/\partial T|_{T \to Tm} = 0$ and solving the resulting quadratic equation for $ID_m$:

(8) $\sqrt{ID_m} = + \frac{A}{2} - C \pm E \cdot \sqrt{[1 + B \cdot (-C + A/4)]}$

The sign of the square root is positive for θ > 0 and negative for θ < 0 and

(9) $A = a^2 b/d^2$
(10) $B = b$
(11) $C = c/d$
(12) $E = a/d$
(13) $a = VTT + \theta_T/\theta_m^2$
(14) $b = -e_m \cdot \sqrt{(8/\beta_m)}$
(15) $c = \theta_T/\theta_m^2$
(16) $d = -[(2\theta_T/\theta_m) - (n/T_m)]/\sqrt{(2\beta_m)}$

Once $ID_m$ is calculated using the above algorithm, $VO_m$ is calculated using Eq. 7 evaluated at $T_m$; that is:

(7a) $VO_m = VT_m - \frac{1}{\theta_m} \cdot (1 - \sqrt{1 - \theta_m \cdot \sqrt{[8 \cdot ID_m/\beta_m]}})$

## 5. p-FET TEMPERATURE EQUATIONS (e = 0)

The equations derived in Section 4, include the θ parameter. Since e is small, it is neglected in this section to gain physical insight into the meaning of the equations.

The p-FET IV characteristics are plotted in Fig. 4 using Eq. 1 with Eqs. 3 and 4 for D = 0 and the parameters listed in the Fig. 4. This figure shows that the so called "temperature independent" point is in fact ill-defined when viewed in detail.

In this analysis, the most important p-FET parameter is VO. Its temperature dependence is analyzed by expressing Eq. 2 as follows:

(17) $VO = VT - \sqrt{2ID/\beta}$

The VO is calculated using Eqs. 3 and 4 for D = 0 and plotted in Fig. 5. These curves show that there is a point at which VO is independent of temperature. This point is determined by differentiating Eq. 17 with respect to temperature and setting the result to zero. This leads to the simple expression for the measurement current:

(18) $ID_m = 2\beta_m^3(-VT_T/\beta_{Tm})^2$

The value for $ID_m$ = 19.2 was calculated using the parameters shown in Fig. 5. The five curves were plotted with ID values that vary by one percent. This shows the effect of missing the target current of $ID_m$. As seen in the figure, the peak in the curve moves to higher temperatures as $ID_m$ increases. The value of VO changes by 0.25 percent for a one percent change in 10.

The temperature sensitivity of VO can be expressed simply by combining Eqs 4, 5, 17, and 18 which leads to:

(19) $VOT = \partial VO/\partial T = VT_T[1 - (Tin/")^{1-n/2}]$

This shows that $VO_T$ = 0 at T = $T_m$ for any n or $VO_T$ = 0 fern = 2 for all T.

The effect of temperature variations on $VO_T$ is analyzed with the help of the horizontal line shown in Fig. 5. This line is 1 mV below the target value of $VO_m$ = -1.5 V. The value of 1 mV was chosen because it is the same magnitude as the dose effects to be measured. The $VO_T$ = -63 μV/°C at point "a" and 63 μV/°C at point "c" seen in Fig. 5. The temperature range between "a" and "c" is more than 70°C. This means that VOT is less than ±63 μV/°C over the 70°C temperature range centered at the measurement temperature, $T_m$. This is a significant improvement in the uncompensated temperature sensitivity of $VT_T$ = 2 mV/°C.

The solution for n = 2 means that the curves

shown in Fig. 5 have zero slope. For this case, the p-FET IV characteristics display a true temperature insensitive point as shown in Fig. 6.

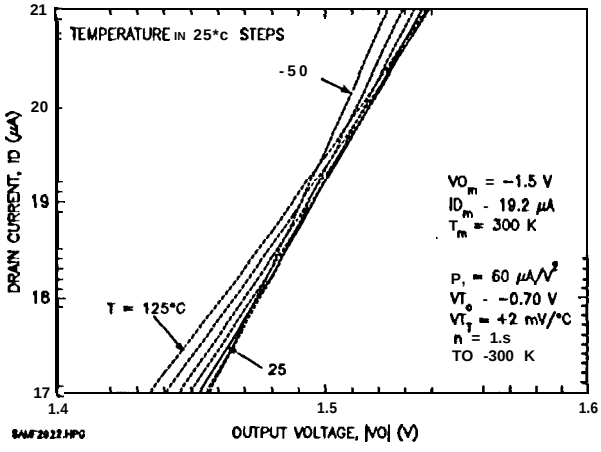


Figure 4. Expanded p-FET IV characteristics showing that the "temperature independent" point is not a point.

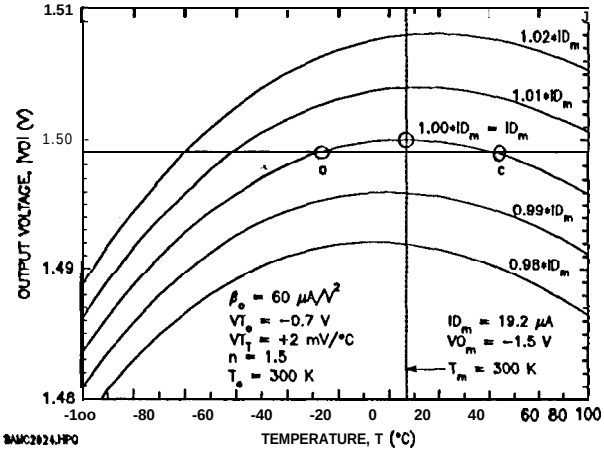


Figure 5. The temperature and current dependence of the p-FET output voltage using Eq. 17.

Next $ID_m$ is analyzed for design purposes by substituting $\beta_m = KP_mW/L$ into Eq. 18; this leads to:

$$(20)\quad ID_m = 2KP_m(VT_T \cdot T_m/n)^2 W/L$$

This equation shows that $ID_m$ depends on the silicon parameters, $KP_m$, $VT_T$, and n, the measurement temperature, $T_m$, and the FET geometry. Thus, once the silicon parameters and $T_m$ are known, the designer is free to choose $ID_m$ by adjusting the W/L ratio.

Finally VO is analyzed for design purposes by substituting Eqs. 5 and 18 into Eq. 17:

$$(21)\quad VO_M = VT_m - 2VT_T \cdot T_m/n$$

This equation shows that $VO_m$ depends on the silicon parameters, $VT_m$, VTT, and n and the measurement temperature, $T_m$. Note that $VO_m$ is independent of FET W/L geometry. Thus the designer has no control over this value. The value for $VO_m$ is about -1.5 V and with irradiation $VO_m$ will become more negative. This is important from an instrumentation stand point. That is, the initial $VO_m$ value must be compensated for by the surrounding circuitry; see Fig. 3.

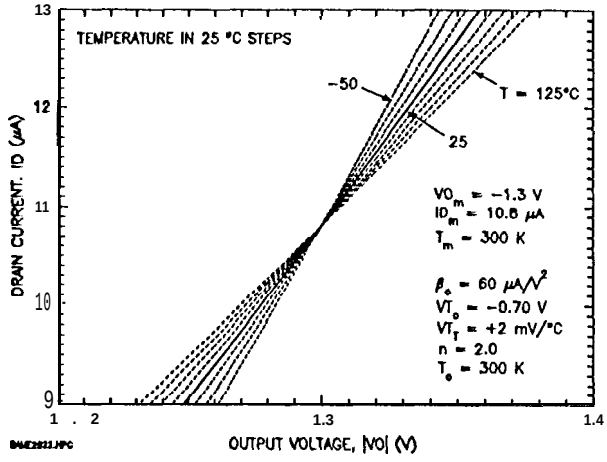


Figure 6. Expanded p-FET IV characteristics showing a true temperature independent point for n = 2.

## 6. p-FET TEMPERATURE DATA ANALYSIS

The p-FETs were measured in packages in an oven using an hp4062 parametric test system. The temperatures are estimated to be accurate to within ±1°C. The measurements were obtained by forcing VO = 2 V and measuring $ID_5$.. Then four additional currents were forced at $\sqrt{ID_1} = 0.2 \cdot \sqrt{ID_5}$, $\sqrt{ID_2} = 0.4 \cdot \sqrt{ID_5}$, $\sqrt{ID_3} = 0.6 \cdot \sqrt{ID_5}$, and $\sqrt{ID_4} = 0.8 \cdot \sqrt{ID_5}$. Once these values are determined they are used throughout the rest of the measurements.

The experimental data, shown in Fig. 7, was fitted using the method of least squares. In the analysis the following parabolic equation was used. The coefficients of the equation were related to the parameters in Eq. 2:

$$(22)\quad \sqrt{ID} = a_0 + a_1 \cdot VO + a_2 \cdot VO^2$$

where

$$(23)\quad a_0 = \sqrt{(\beta/2)} \cdot VT \cdot (1 - \theta \cdot VT/2)$$
$$(24)\quad a_1 = -\sqrt{(\beta/2)} \cdot (1 - \theta \cdot VT)$$
$$(25)\quad a_2 = -\sqrt{(\beta/2)} \cdot \theta/2.$$

The "a" parameters are used to obtain VT, β,

and θ for each IV curve. The VT solution was obtained using VO = VT at ID = O. This leads to a quadratic equation whose solution is:

(26) $VT = a_1/(2a_2) \cdot (-1+\sqrt{1-4a_0a_2/a_1^2})$

The sign of the square root is positive. This can be verified by setting El = O or $a_2$ = O. The solution for B is:

(27) $B = 2(a_1 + 2a_2 \cdot VT)^2$

The solution for θ is:

(28) $\theta = 2a_2/(a_1 + 2a2\ VT)$

The IV points, shown in Fig. 7, were fitted using the above procedure. The B, VT, and θ values are listed in Table 1 for three temperatures.

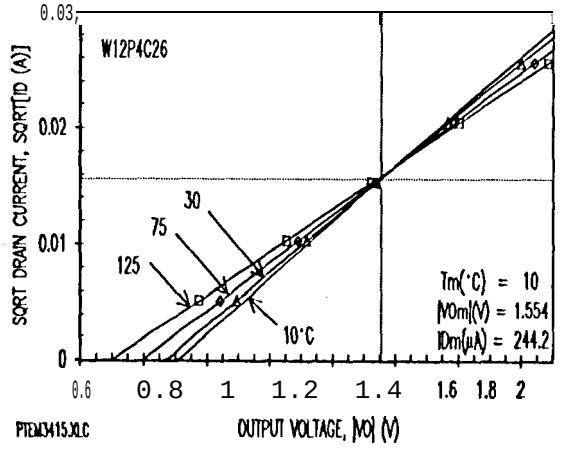


Figure 7. 1.2-μm CMOS p-FET IV temperature response for flight p-FET W12P4C26.

Using the data listed in Table 1, the temperature parameters for VT and θ were extracted by least squares fitting this data using Eqs. 3 and 6. The temperature parameter for 13 was extracted using Eq. 4 after it was linearized by taking the logarithm. The temperature parameters are listed in Table 2.

Values for $ID_m$ and $VO_m$ were calculated using Eqs. 7a and 8 and the parameters listed in Table 2. The results are listed in Table 2 and plotted in Fig. 7.

Table 1. Flight p-FET4 parameters (W12P4C26)

| T °C | VT V | β mA/V² | θ 1/V |
|---|---|---|---|
| 30 | -0.874 | 1.100 | 0.056 |
| 75 | -0.800 | 0.891 | 0.041 |
| 125 | -0.703 | 0.708 | 0.027 |

Table 2. Flight p-FET Parameters (T. = 20°C, $T_m$ = 10"C, W12P4C26)

| PARAM | UNITS | MEAN STDEV |
|---|---|---|
| W | urn | 182 |
| L | urn | 4 |
| AL | urn | 0.3459 |
| $VT_o$ | V | -0.8944*0.0055 |
| $VT_T$ | mV/°C | 1.8002%0.0800 |
| $β_O$ | mA/V² | 1.1667*0.0126 |
| $KP_o$ | μA/V² | 25.6421*0.2774 |
| n | -- | 1.6139*0.0528 |
| $β_{To}$ | (μA/V²)/°C | -6.4231 |
| $θ_O$ | 1/V | 0.0593±0.0014 |
| $θ_T$ | (1/kV)/°C | -0.3153*0.0209 |
| $VT_m$ | V | -0.9125 |
| $β_m$ | mA/V² | 1.2339 |
| $θ_m$ | 1/V | 0.0624 |
| $β_{Tm}$ | (μA/V²)/°C | -7.0370 |
| $I D_m$ | μA | 244.2 |
| VOm | V | -1.554 |

## 7. p-FET DOSE DATA ANALYSIS

The p-FET dose dependence was determined using Cobalt-60 irradiation. The devices were irradiated with their lids on, at room temperature, at 1 rad/sec, and at zero bias. The p-FETs were measured "within 15 minutes after Cobalt-60 irradiation.

The p-FET irradiation results, shown in Fig. 8, were fitted using Eq. 22. This produced a set of VT, β, and θ values for each dose value. These values are plotted in Figs. 9 to 11 for four p-FETs. The radiation results are listed in Table 3 for one of the p-FETs.

The VT values, plotted in Fig. 9, show a high degree of linearity during irradiation and a slight recovery with annealing, The group average slope of the VT vs dose curve is VTD = -1.698±0.038 mV/krad(Si). The shift in VT with radiation is consistent with the build up of positive oxide charge and interface states. The slight recovery of VT during room temperature anneal is consistent with

Table 3. Ground Test p-FET Cobalt-60 Radiation Parameters W12P4C05

| PAR. | UNITS | MEAN STDEV |
|---|---|---|
| VTD | mV/krad(Si) | -1.674±0.004 |
| $\beta_D$ | $\mu A/V^2/krad(Si)$ | -3.585*0.164 |
| $KP_D$ | $\mu A/V^2/krad(Si)$ | -0.079*0.004 |
| $\theta_D$ | 1/kV/krad(Si) | -1.184*0.018 |
| $VO_{Dm}$ | mV/krad(Si) | -2.591±0.018 |

C:\XL\XLS\PDos3711.HPG;32 p10;26 p10;HPGL
Figure 8. 1.2-$\mu$m CMOS p-FET IV dose/anneal response for p-FET W12P4C05.

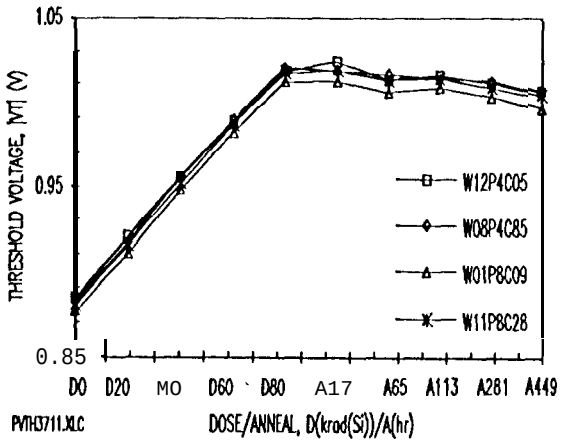


Figure 9. Four 1.2-$\mu$m CMOS p-FET threshold voltage dose/anneal responses. "

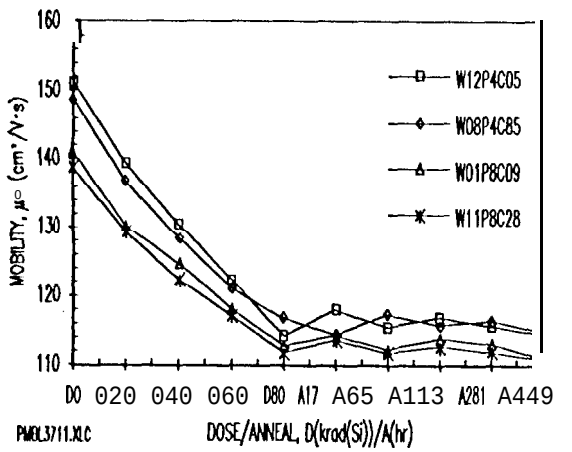


Figure 10. Four 1.2-$\mu$m CMOS p-FET hole mobility dose/anneal responses.

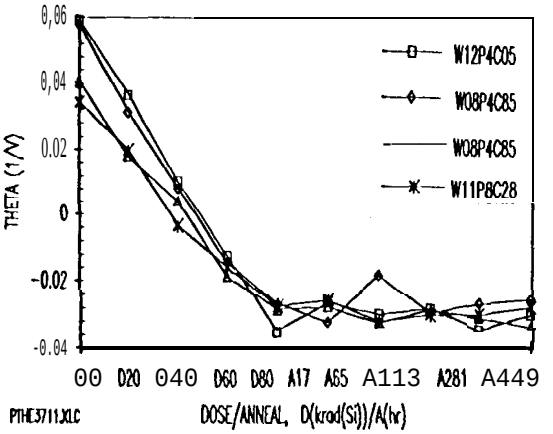


Figure 11. Four 1.2-$\mu$m CMOS p-FET theta dose/anneal responses.

the slight loss of oxide charge. The interface states appears to be stable as seen by the stability of the mobility during anneal.

The $\beta$ values were converted to zero-field hole channel mobility using:

$$(29)\ \mu_0 = (L - \Delta L) \cdot \beta / (W \cdot C_0)$$

In this analysis the value for Co was calculated using the MOSIS supplied value for the gate-oxide thickness of 21.8-nm oxide.

The data, shown in Figure 10, are clustered according to the p-FET's W/L ratios. The $\mu_0$ is stable after annealing. The build up of positively charged interface states during irradiation degrades the mobility due to increase in channel scattering centers. Since the mobility does not anneal at room temperature, the interface states are stable.

The $\theta$ values, shown in Fig. 11, are clustered according to the p-FET W/L ratios. The characteristics show no annealing indicating that the interface density is stable. The $\theta$ represents the curvature term for the parabolic equation given in Eq. 2. The curvature is difficult to see in Fig. 8 because $\theta$ is very small. As seen in Fig. 11, $\theta_{max} = 0.06$ 1/V. It's influence in Eq. 2 is less than 3 percent because it enters as $\theta/2$. This justifies the Taylor Series expansion used in the simplification leading to Eq. 2.

Notice that $\theta$ is positive initially and negative after irradiation and anneal. The sign of $\theta$ indicates the direction of the $\sqrt{ID}$ vs VO parabola used to fit the data. For $\theta > 0$ the parabola points down and for $\theta < 0$ the parabola points up. For $\theta = 0$, the $\sqrt{ID}$vsVO curve is a straight line.

## 8. DOSIMETRY

The device dose sensitivity is derived in this section. Since the dose is measured at the constant current, $ID_m$, the radiation dose sensitivity of VO is greater than VTD. This is evident in Fig. 8 where the spread in the curves is wider at ID = $ID_m$ than at ID = O due to B's or mobility dose dependence.

In this section the output-voltage dose

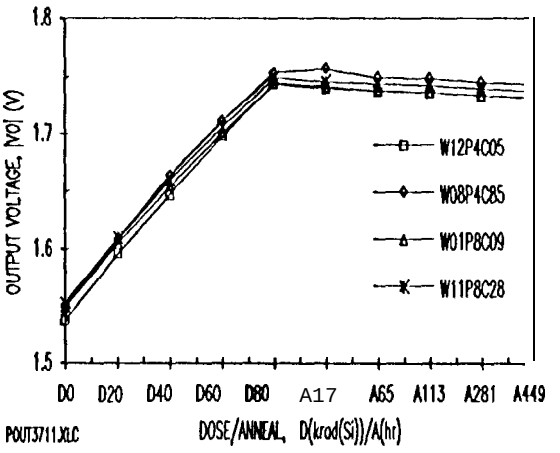


Figure 12. Four 1.2-$\mu$m CMOS p-FET output voltage dose/anneal responses where the current is at $ID_m$ where $T_m$ = 10"C.

sensitivity, VOD, for $\theta$ = O is calculated by differentiating Eq. 17 with respect to dose at ID = ID. Then $ID_m$, given in Eq. 18, is substitute into the result. The output-voltage dose sensitivity is:

$$(30)\quad VO_{Dm} = \partial VO/\partial D|_{Tm} = VTD - VT_T \cdot \beta_D/\beta_{Tm}$$

A value for $VO_{Dm}$ = -2.59 mV/krad(Si) was calculated using the values listed in Tables 2 and 3. This result is considerably larger than VTD = -1.67 mV/krad(Si).

The output voltage for the four p-FET samples is shown in Fig. 12. This plot was obtained from data sets like those shown in Fig. 8 where the VO values were obtained at $ID_m$. The data shows a nearly linear rise in Vo with dose and a slight annealing effect.

The similarity of the data is remarkable considering the p-FET samples came from different wafers from the same run. This means that the sample set can be assumed to be uniform and that the results can be used to calibrate the flight parts which, of course, can not be irradiated on the ground.

For the circuitry shown in Fig. 3, which uses an 8-bit ADC to span 100 krad(Si), the resolution is 100k/256 = 390 rad(Si)/bit. This means that the p-FET dosimeter can easily resolve a krad(Si) of dose.

## 9. CONCLUSION

The use of on-chip p-FET dosimeters has been established and provides a radiation sensitivity of -2.6 mV/krad(Si) for the 1.2-$\mu$m CMOS used in this study. The temperature dependence is less the ±63 $\mu$V/°C over the temperature range of 70°C centered about the p-FET temperature independent point. The use of on-chip p-FETs provides a direct measure of the radiation dose experienced by the associated CMOS IC.

REFERENCES:


1. A. Holmes-Siedle, "The space-charge dosimeter - General principles of a new method of radiation detection," Nucl. Instr. & Methods, Vol. 121, 169-179 (1974).

2. E. G. Stassinopoulos, V. Danchenko, R. A, Cliff, M. Sing, G. J. 8rucker, and R. S. Ohanian, "Prediction and measurement results of radiation damage to CMOS devices on board spacecraft," IEEE Trans. Nucl. Sci., NS-24, 2289-2293 (1977).

3. A. Holmes-Siedle, L. Adams, S. Marsden, and 8. Pauly, "Calibration and flight testing of a low-field pMOS dosimeter," IEEE Trans. Nucl. Sci., NS-32, 4425-4429 (1985).

4. G. A. Soli, 8. R. Blaes, and M. G. Buehler "CRRES microelectronic test chip orbital data 11," IEEE Trans. Nucl. Sci., NS-39, 1840-1845 (1992) .

5. A. Holmes-Siedle, L. Adams, G. Ensell, "MOS dosimeters - Improvement of responsivity, " RADECS91, 65-69 (1991).

6. M. O'Sullivan, A. Kelleher, J. Ryan, B. O'Neill, and B. Lane, "Temperature compensation of PMOS dosimeters," Proc. ESA Electronics Components Conf., ESTEC, 281-285 (November 1990).

7. Y.P. Tsividis, Operation and Modeling of the MOS Transistor, McGraw-Hill [New York, 1987) .

8. M. G. Buehler, B. R. Blaes, and Y-s. Lin, "Radiation dependence of inverter propagation delay from timing sampler measurements," IEEE Trans. on Nuclear Science, Vol 36, 1981-1989 (1989) .

ACKNOWLEDGMENTS :

The research described herein was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the Ballistic Missile Defense Organization, Innovative Science and Technology Office. The RADMON was designed for use on the STRV (Space Technology Research Vehicle) to be launched in 1994. The authors are indebted to MOSIS for brokering the CMOS fabrication and to one of the reviewers who pointed out that this is the first time a p-FET dosimeter has been fabricated in the fine-line, thin-oxide semiconductor technology. File: NSRE3625.DOC